Tested at 2.7ns/66

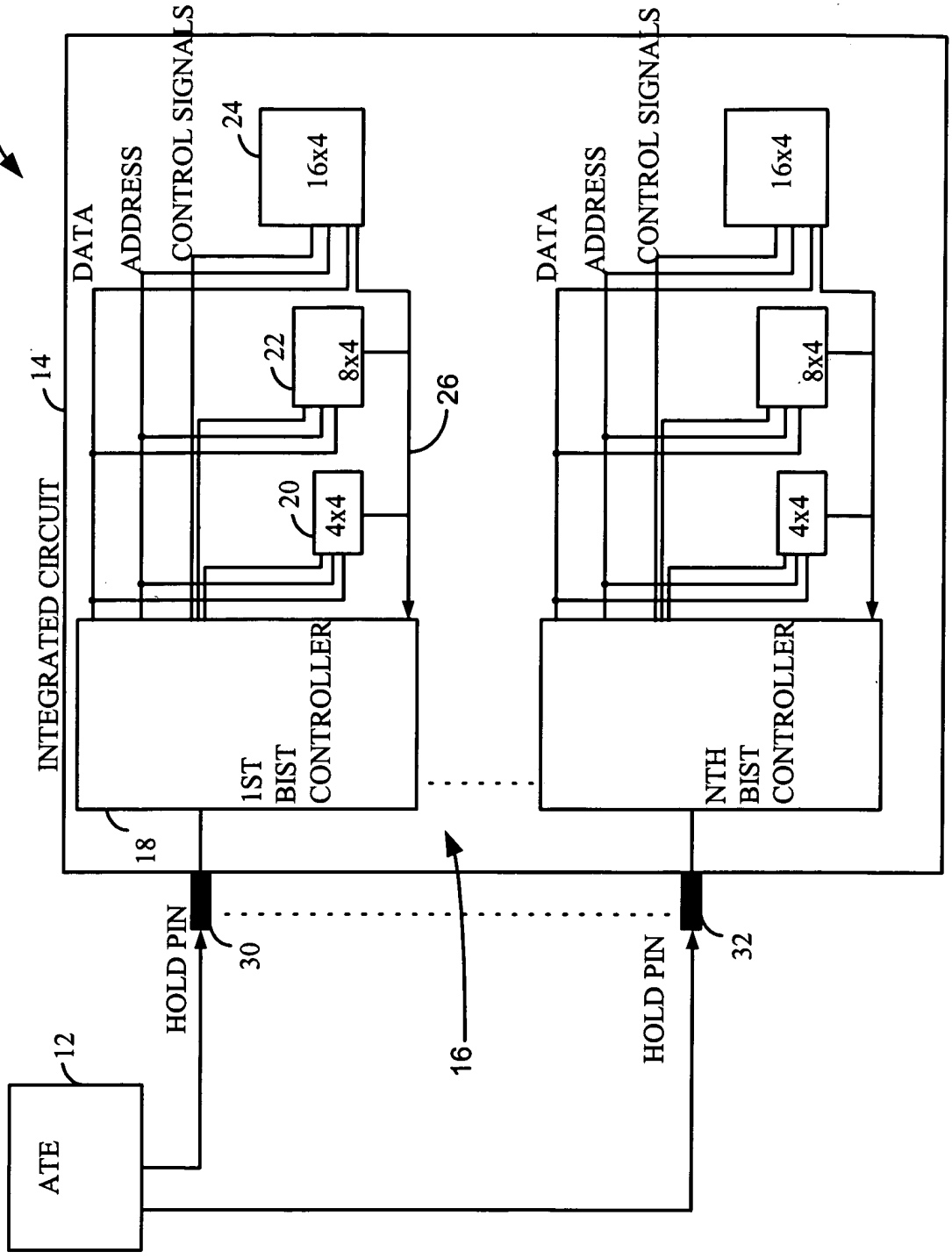
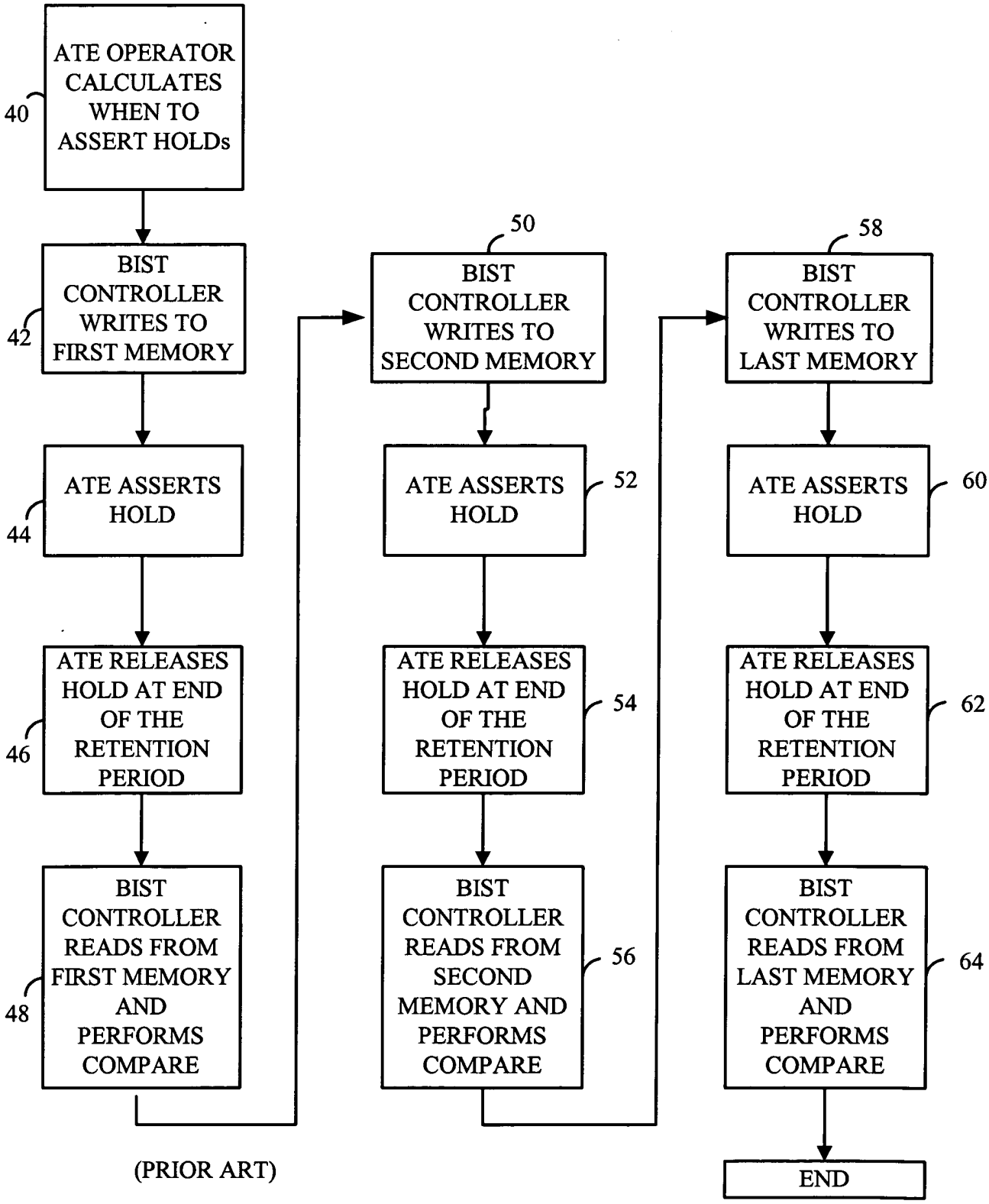


FIG. 1
(PRIOR ART)

FIG. 2

TEST ON THREE MEMORIES COUPLED TO A SINGLE SEQUENTIAL BIST CONTROLLER USING THREE SEPARATE IDLE PERIODS



(PRIOR ART)

EXPRESS MAIL NO. EL524256869

FIG. 3

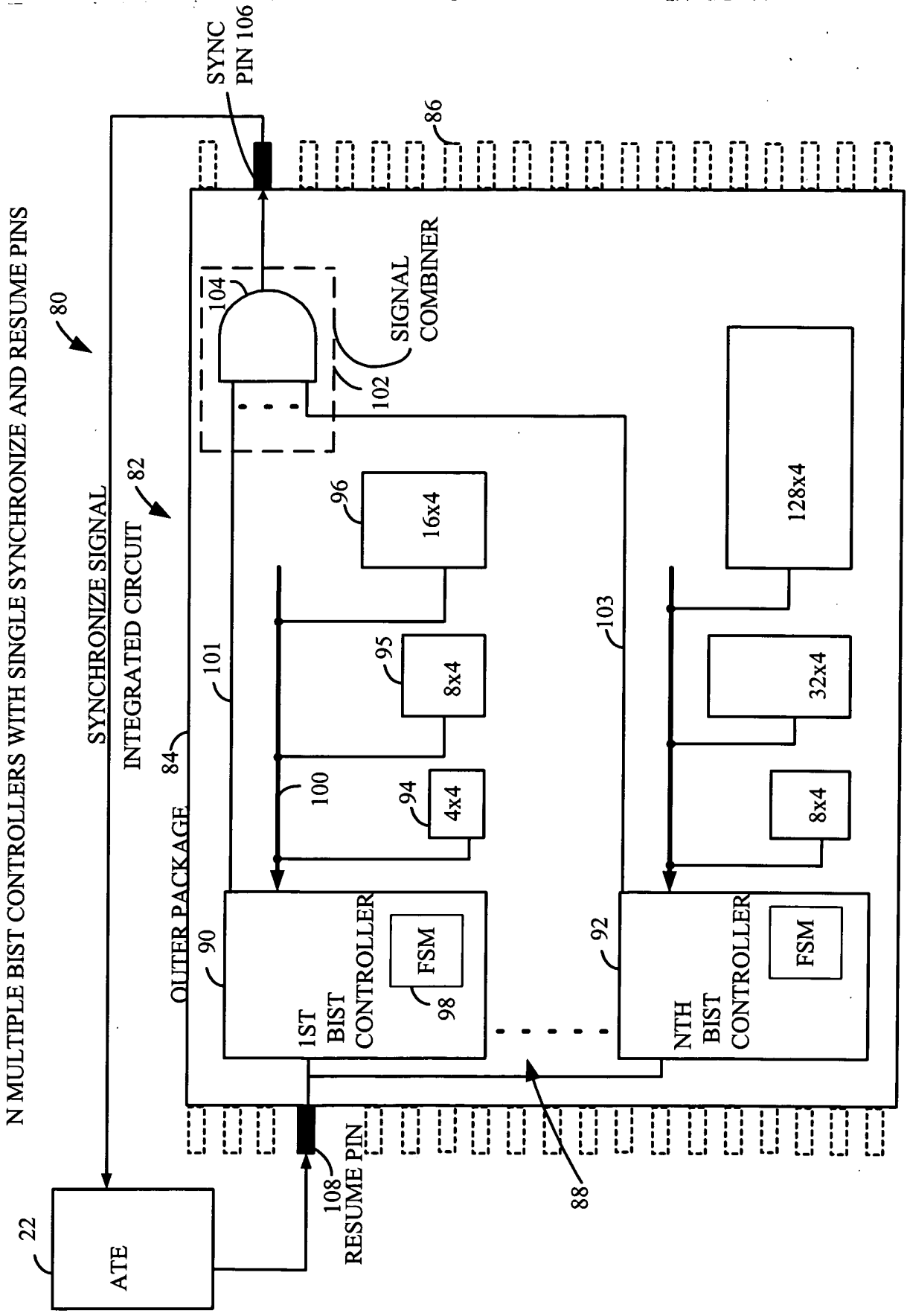


FIG. 4

TEST OF MEMORIES WITH MULTIPLE PARALLEL BIST CONTROLLERS USING SYNCHRONIZATION STATE

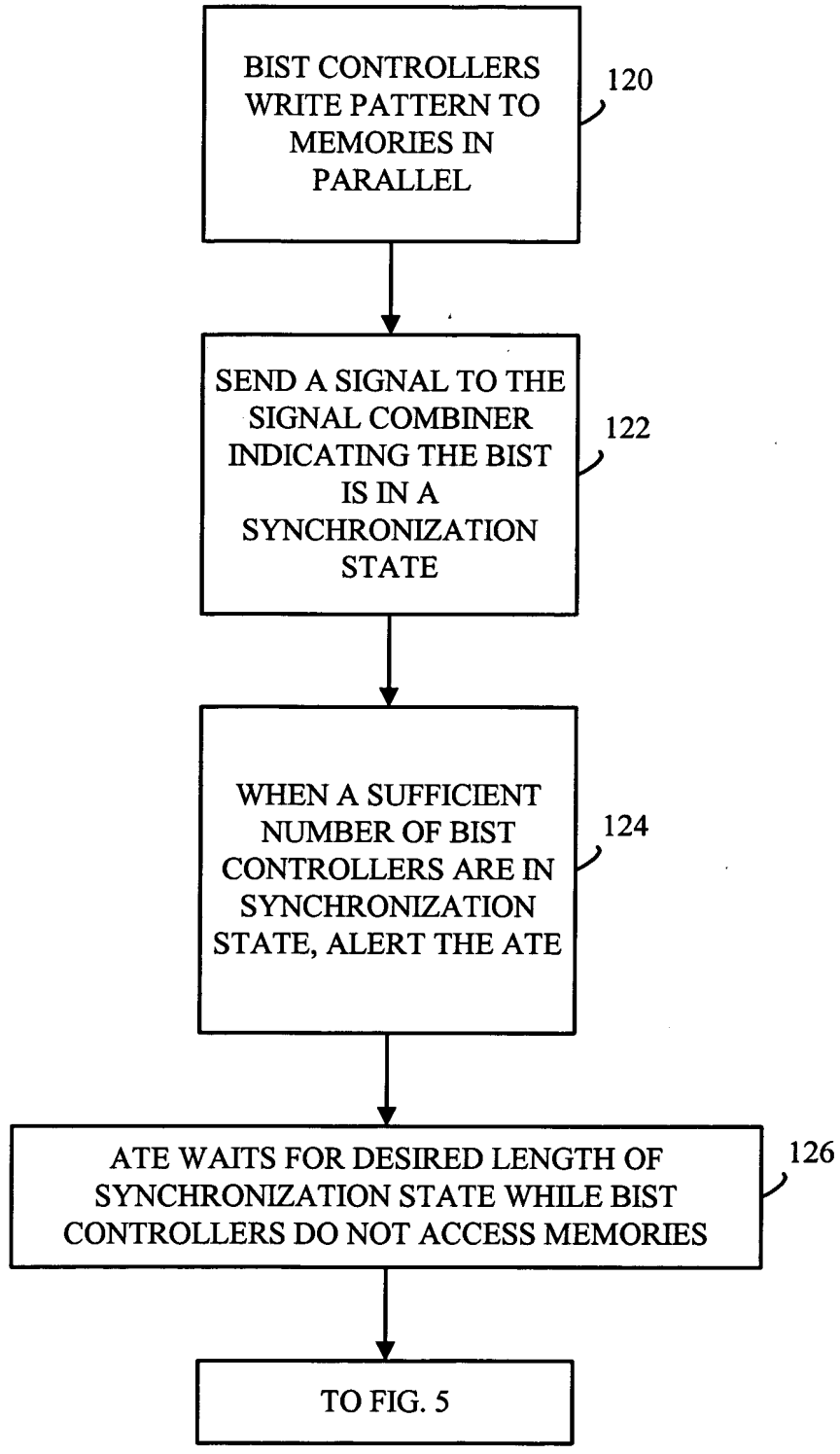


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FIG. 5

TEST OF MEMORIES WITH MULTIPLE PARALLEL BIST CONTROLLERS USING SYNCHRONIZATION STATE (CONTINUED)

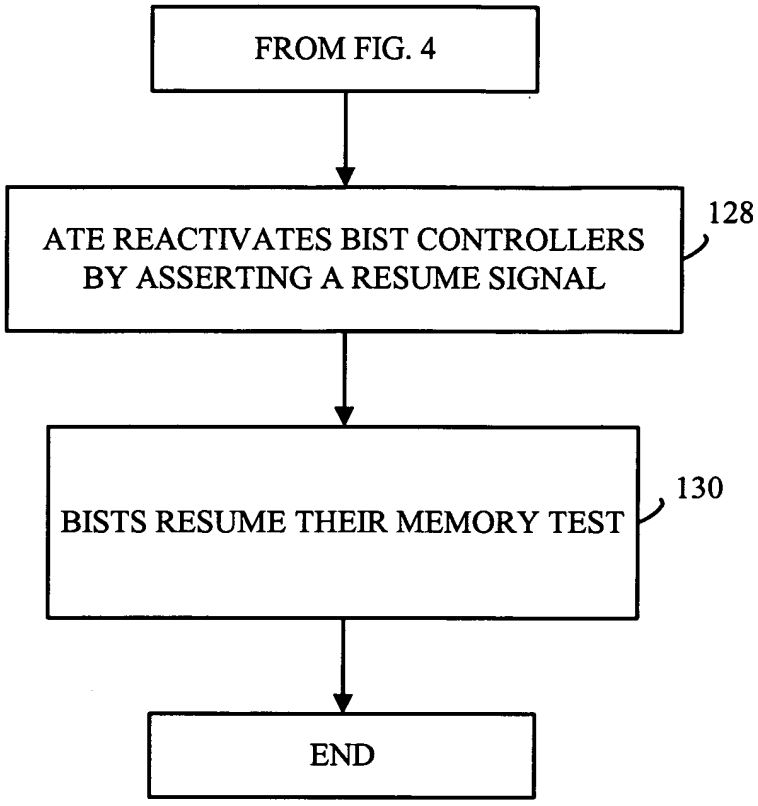

FIG. 6

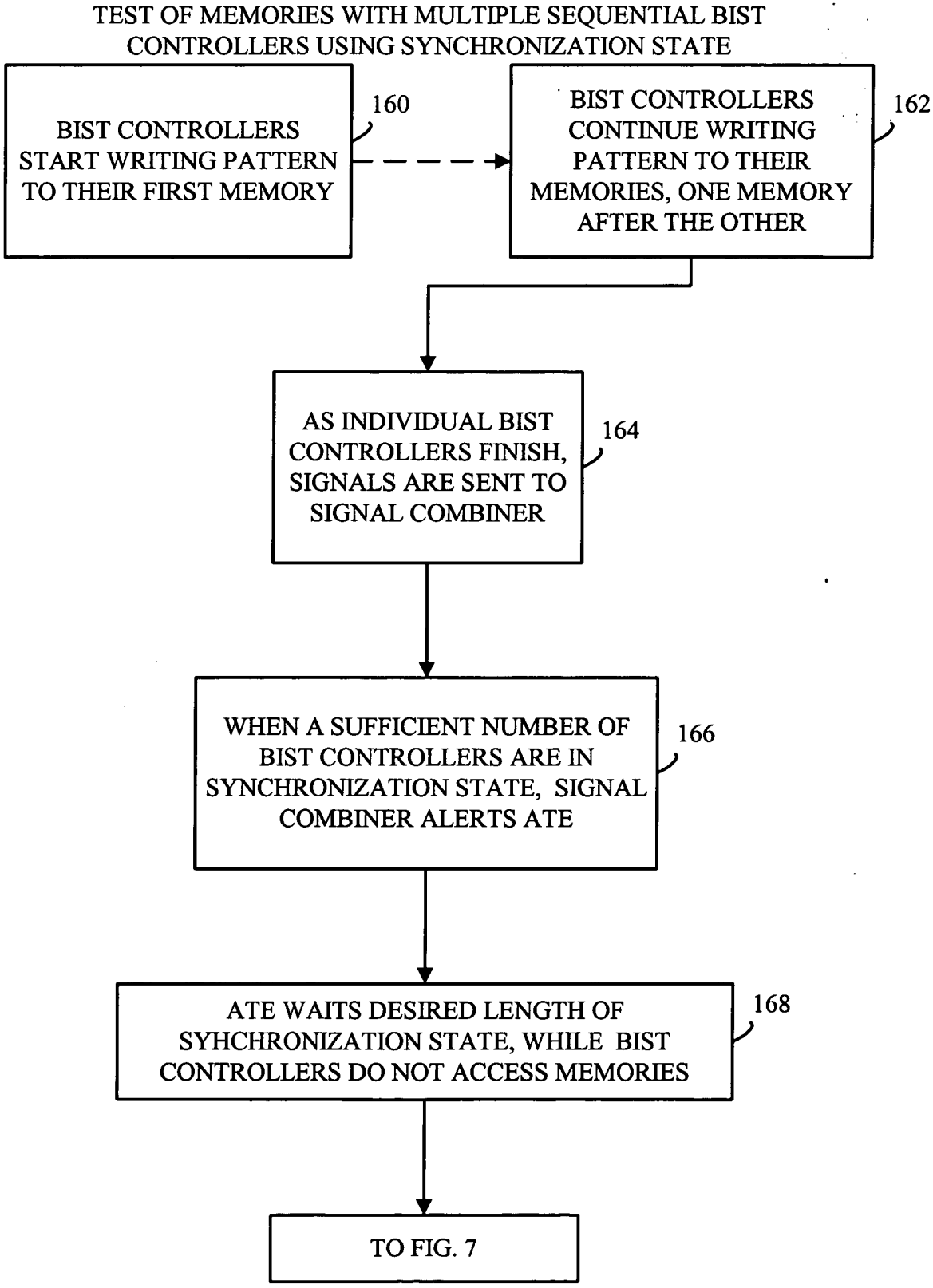

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FIG. 7

TEST OF MEMORIES WITH MULTIPLE SEQUENTIAL BIST CONTROLLERS USING SYNCHRONIZATION STATE (CONTINUED)

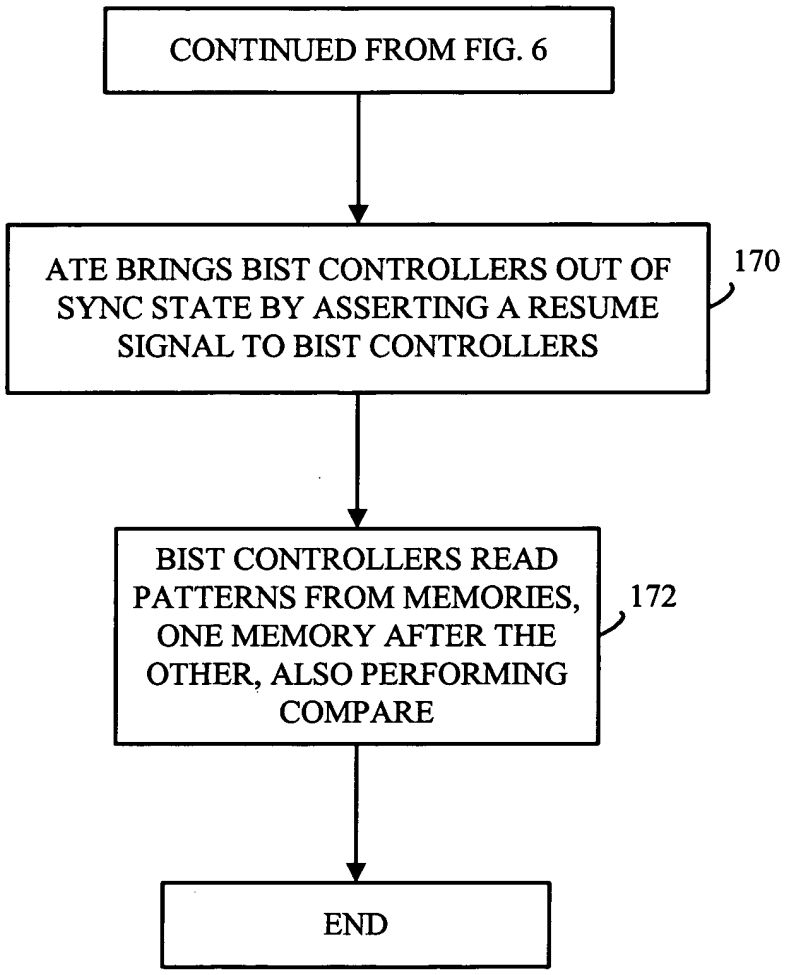

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FIG. 8 — BIST CONTROLLER GENERATOR

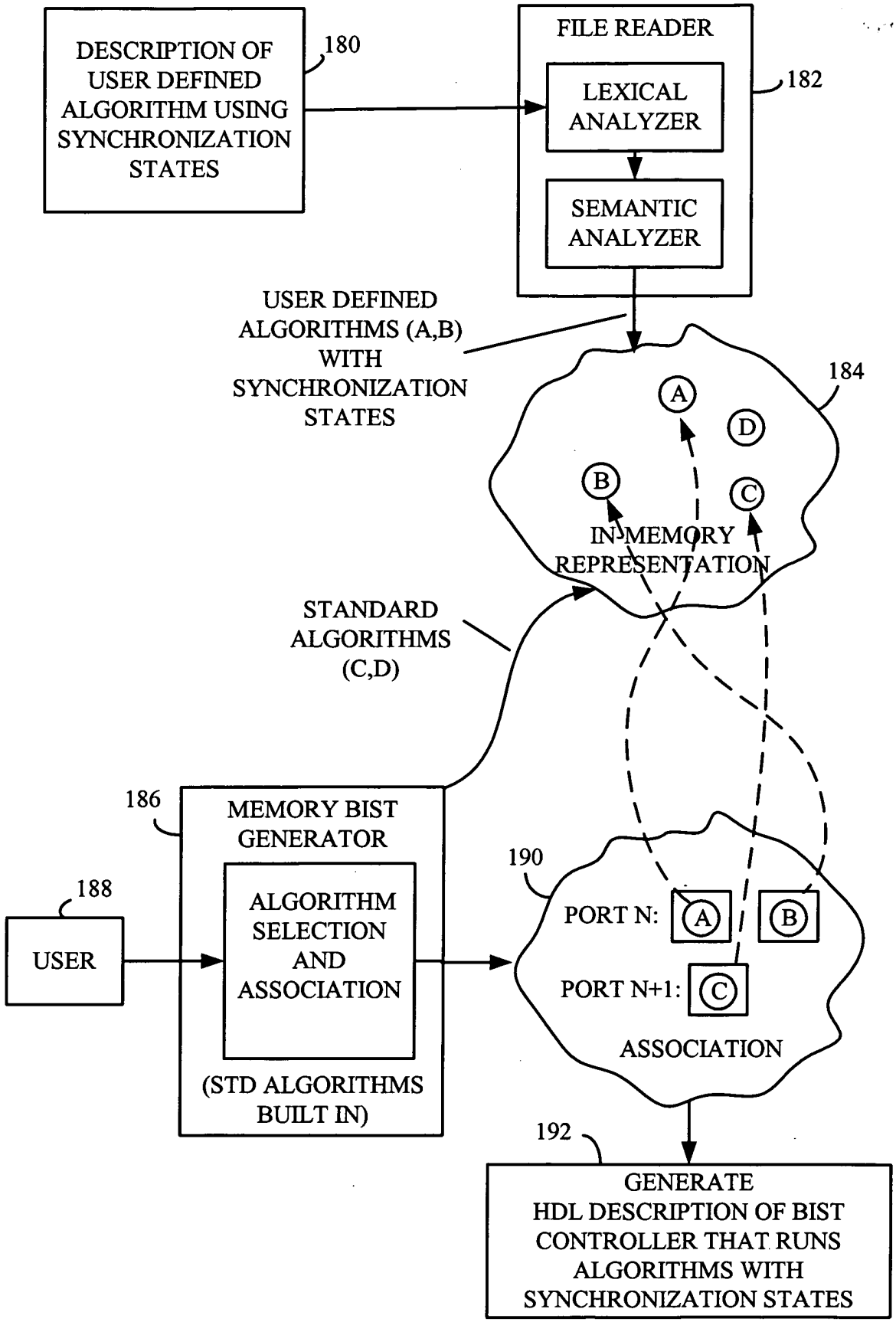
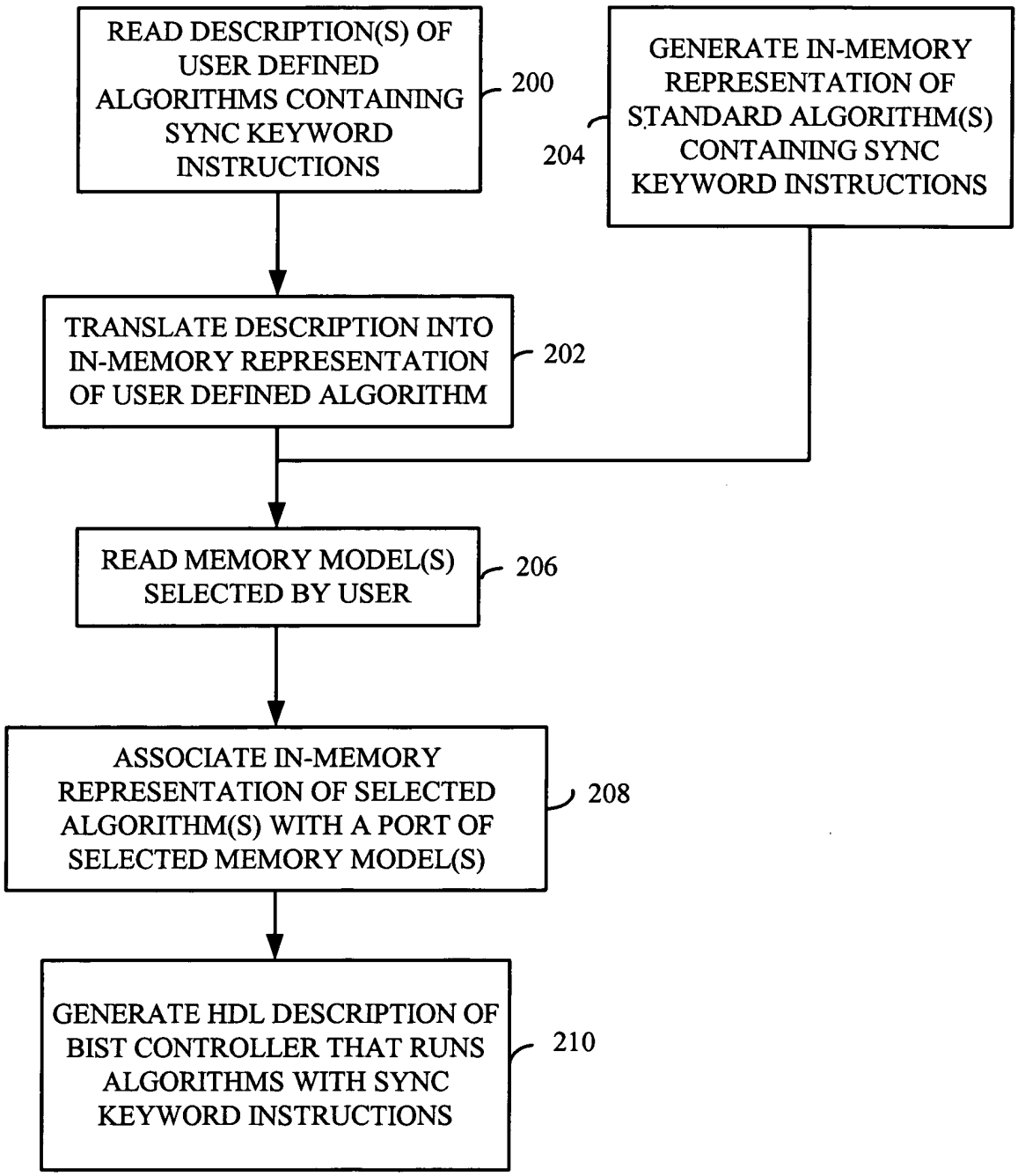


FIG. 9

GENERATING A BIST CONTROLLER THAT RUNS USER DEFINABLE ALGORITHIMS WITH SYNC KEYWORD